AMENDMENTS TO THE CLAIMS

Claim 1. (Currently amended) An integrated input/output controller integrated into a single integrated circuit device for transceiving data as a plurality of data blocks between at least one host and a disk array, comprising:

a host interface subsystem coupled to at least one host for receiving host commands and tranceiving ~~and to transceive~~ said data blocks with the ~~at least one~~ host in response to the host commands, said host interface system including a command decode controller for parsing host commands to identify data flow type host commands and non data flow type commands;

a RAID mapping controller, coupled to the host interface subsystem, for mapping logical block addresses of the data flow type host commands into disk ~~peripheral~~ block addresses of a plurality of ~~one or more~~ disks of a RAID disk array; ~~peripherals;~~ and

a disk ~~peripheral~~ interface subsystem, coupled to said plurality of ~~one or more~~ disks of said disk array, ~~peripherals~~ for transceiving said data blocks with the plurality of ~~one or more~~ disks ~~peripherals~~ using the disk ~~peripheral~~ block addresses generated by the mapping controller;

wherein,

for each data flow type host command,

said command decode controller communicates an associated logical block address to the mapping controller,

said mapping controller converts the associated logical block address to an associated disk ~~peripheral~~ block address, and

said disk ~~peripheral~~ interface subsystem accesses the plurality of ~~one or more~~ disks ~~peripherals~~ using said associated disk ~~peripheral~~ block address.

Claim 2. (canceled)

Claim 3. (withdrawn) The integrated input/output (I/O) controller of claim 1, wherein:

said host commands are high level I/O commands received from a host;

said command decode controller includes circuits for parsing the high level I/O commands to determine whether to read or write data;

said mapping controller includes circuits for mapping the high level I/O request into one or more peripheral I/O commands, the one or more peripheral I/O commands indicating which of the one or more peripherals and which respective data locations are to be accessed; and

said peripheral interface subsystem includes circuits for servicing the high level I/O request by reading or writing data between the host and the one or more peripherals using the respective data locations.

Claim 4. (withdrawn) The integrated I/O controller of claim 3, further including circuits to perform: prior to servicing the high level I/O request, storing data temporarily into an external cache buffer from the data flow between the host and the one or more disks ~~peripherals~~.

Claim 5. (withdrawn) The integrated I/O controller of claim 3, wherein each of the one or more peripheral I/O commands further indicates the number of blocks of data to be serviced.

Claim 6. (withdrawn) The integrated I/O controller of claim 3, wherein said mapping controller includes circuits to perform:

parsing a high level command from an I/O request packet,

decoding the high level command and generating a range operation request in response thereto, and

generating the one or more peripheral I/O commands in response to the range operation request.

Claim 7. (withdrawn) The integrated I/O controller of claim 3, wherein ~~each of the one or more peripherals are storage disks and~~ each of the one or more peripheral I/O commands are Small Computer System Interface (SCSI) disk I/O commands.

Claim 8. (withdrawn) The integrated I/O controller of claim 3, wherein the high level I/O command is a command of a Small Computer System Interface (SCSI) Command Descriptor Block (CDB) standard.

Claim 9. (withdrawn) The integrated I/O controller of claim 3, wherein the circuits of the integrated I/O controller are hard wired circuits.

Claim 10. (withdrawn) The integrated I/O controller of claim 3, wherein the circuits of the integrated I/O controller are microcoded circuits and state machines operating concurrently.

Claim 11. (withdrawn) The integrated I/O controller of claim 3, wherein the circuits of the integrated I/O controller are hard wired circuits, microcoded circuits and state machines operating concurrently.

Claim 12. (withdrawn) The integrated I/O controller of claim 3, wherein the circuits of the integrated I/O controller are programmable micro-controllers operating concurrently.

Claim 13. (canceled)

Claim 14. (withdrawn) The integrated input/output controller of claim 1, further comprising a micro-controller subsystem coupled to the host interface subsystem for processing non data flow type host commands

Claim 15. (withdrawn) The integrated input/output controller of claim 1, further comprising:

a cache manager coupled to the host interface subsystem and the peripheral interface subsystem, the cache manager to manage entries in a cache buffer to temporarily store data of the data flow between the disk ~~peripheral~~ and the host.

Claim 16. (withdrawn) The integrated input/output controller of claim 15, further comprising:

a buffer manager coupled to the host interface subsystem, the peripheral interface subsystem, and the cache manager, the buffer manager to manage data storage in the cache buffer.

Claim 17. (canceled)

Claim 18. (withdrawn) The integrated input/output controller of claim 1, wherein the host interface subsystem includes a host exchange controller to control the physical connection and protocol of the host.

Claim 19. (canceled)

Claim 20. (withdrawn) The integrated input/output controller of claim 1, wherein the disk ~~peripheral~~ interface subsystem includes a disk ~~peripheral~~ exchange controller to control the physical connection and protocol of the disk ~~peripheral~~.

Claim 21. (withdrawn) The integrated input/output controller of claim 1, wherein the disk ~~peripheral~~ interface subsystem includes a Fibre channel disk port to transceive data with the disk ~~peripheral~~ using a Fibre channel protocol.

Claims 22-27. (canceled)

Claim 28. (withdrawn) The integrated input/output controller of claim 1, further comprising:

a micro-controller coupled to the host interface subsystem, the micro-controller to perform initialization and handle error and exception handling events.

Claim 29. (withdrawn) The integrated input/output controller of claim 28, wherein the host interface subsystem includes a fibre channel host port to transceive data with the at least one host using a fibre channel protocol.

Claim 30. (canceled)

Claim 31. (withdrawn) The integrated input/output controller of claim 1, wherein the command decode controller further validates a host command and initiates execution of the host command by the integrated input/output controller.

Claim 32. (withdrawn) The integrated input/output controller of claim 1, wherein the command decode controller maintains a command queue for each volume accessible by the at least one host to further validate a host command and to queue the host command for execution.

Claim 33. (withdrawn) The integrated input/output controller of claim 1, wherein the command decode controller further validates a host command and, if the host command is determined to be invalid, the host command is passed to a micro-controller subsystem for processing as a non data flow command.

Claim 34. (withdrawn) The integrated input/output controller of claim 1, wherein the host commands are high level input/output requests.

Claim 35. (canceled)

Claim 36. (canceled)

Claim 37. (withdrawn) The integrated input/output controller of claim 1 ~~36~~, wherein the one or more disks of the at least one array of disks are magnetic storage media, optical storage media or semiconductor storage media.

Claim 38. (withdrawn) The integrated input/output controller of claim 1 ~~36~~, wherein the disk interface subsystem includes one or more fibre channel disk ports to transceive data with the one or more disks of the at least one disk array using a fibre channel protocol.

Claim 39. (canceled)

Claim 40. (withdrawn) The integrated input/output controller of claim 28, wherein the mapping controller is programmable hardware to flexibly control the mapping of blocks of data storage on the one or more disks of the at least one disk array.

Claim 41. (withdrawn) The integrated input/output controller of claim 28, wherein the mapping controller receives a requested command input packet to generate expanded command output packets in response thereto, the requested command input

packet functions as a logical address and the expanded command output packets function as physical addresses.

Claim 42. (withdrawn) The integrated input/output controller of claim 28, further comprising:

a buffer manager and a cache manager, the buffer manager and the cache manager being coupled to a cache buffer and a cache table buffer respectively to flexibly control the reading and writing of data to and from the mapped data storage on the one or more disks of the at least one disk array.

Claim 43. (canceled)

Claim 44. (canceled)

Claim 45. (canceled)

Claim 46. (canceled)

Claim 47. (withdrawn) The integrated input/output (I/O) controller of claim 1, further comprising:

a mapping engine to map high level host I/O requests into low level I/O commands; and

a low level command manager to manage data read and data write accesses into and out of a disk ~~peripheral device~~ in response to the low level I/O commands.

Claim 48. (withdrawn) The integrated input/output (I/O) controller of claim 47, further comprising:

a buffer manager to arbitrate access by the one or more servers and to control data reads and data writes into and out of a buffer memory.

Claim 49. (withdrawn) The integrated input/output (I/O) controller of claim 47, further comprising a micro-controller to handle non-data flow commands, system initialization and error handling exception conditions.

Claim 50. (canceled)

Claims 51-52. (canceled)

Claim 53 (Currently amended) The controller of claim 1, wherein the data flow type host commands comprise read and write commands.

Claim 54 (withdrawn): The controller of claim 1, further comprising a cache manager for communicating with a cache memory.

Claim 55 (withdrawn) The controller of claim 54, wherein said cache manager determines whether data corresponding to said associated logical block address is stored in the cache memory before said command decode subsystem communicates said associated logical block address to said mapping controller, and if data corresponding to said logical block address is stored in the cache memory, said host command is processed using said cache memory and said command decode subsystem does not communicate said associated logical block address to said mapping controller.

Claim 56 (withdrawn): The ~~An~~ integrated input/output controller of claim 15, wherein ~~integrated into a single integrated circuit device, comprising~~:

~~a microcontroller subsystem for processing non data flow type host commands; and~~

~~a data flow subsystem for processing data flow type host commands, said data flow subsystem comprising,~~

~~a mapping controller for translating a logical block addresses of data flow type commands to peripheral block addresses;~~

~~a peripheral interface subsystem for accessing at least one peripheral;~~

~~a host interface subsystem comprising:~~

said ~~a~~ host exchange controller maintains ~~for maintaining~~ a host exchange table comprising a plurality of table entries, receiving a host command, adding a new table entry to said host exchange table corresponding to said host command, each table entry being associated with a tag, and outputting the tag associated with the new table entry; and

said ~~a~~ command decode controller maintains ~~for maintaining~~ a command queue comprising a plurality of queue entries, receiving the tag associated with the new table entry, adding a new queue entry corresponding to said tag, and outputting a cache manager packet; and

said ~~a~~ cache manager subsystem manages ~~for managing~~ a cache memory, wherein said cache manager subsystem:

receiving the cache manager packet, if data associated with said cache manager packet is stored in the cache memory;

forwarding read data from the cache to the host exchange controller if the host command is a read command;

accepting write data from the host exchange controller if the host command is a write command; and

if data associated with said cache manager packet is not stored in the cache memory, forwarding a logical block address associated with said cache manager packet to the mapping controller to receive an associated disk ~~peripheral~~ block address, said disk

~~peripheral~~ interface subsystem accessing at least one disk ~~peripheral~~ using said associated disk peripheral block address.

Claim 57 (withdrawn): The integrated input/output controller of claim 56, wherein data flow host commands comprise read and write commands.

Claim 58 (withdrawn): The integrated input/output controller of claim 56, wherein said mapping controller is capable of accepting a logical block address for a virtual volume which spans a plurality of disks ~~peripherals~~ and translating said logical block address to an associated disk ~~peripheral~~ block address.

Claim 59 (new): The integrated input/output controller of claim 1, wherein said disk interface subsystem also transceives at least one additional block when said disk interface subsystem transceives said data block with said plurality of disks.

Claim 60 (new): The integrated input/output controller of claim 59, wherein said at least one additional block comprise parity information regarding at least said data block.

Claim 61 (new): The integrated input/output controller of claim 59, wherein said at least one block comprises a copy of said data block.

Claim 62 (new): The integrated input/output controller of claim 1, wherein said mapping controller converts the associated logical block address to an associated disk block address in accordance with a mapping which stripes data across said plurality of disks.

Claim 63 (new): The integrated input/output controller of claim 1, wherein said mapping controller converts the associated logical block address to an associated disk block address in accordance with a mapping which mirrors data across said plurality of disks.

Claim 64 (new): The integrated input/output controller of claim 1, wherein said mapping controller converts the associated logical block address to an associated disk block address in accordance with a mapping which mirrors and stripes data across said plurality of disks.

Claim 65 (new): The integrated input/output controller of claim 1, wherein said disk interface subsystem comprises a SCSI initiator.

Claim 66 (new): The integrated input/output controller of claim 1, wherein said disk array is organized as a plurality of logical volumes and said controller independently processes commands directed said plurality of logical volumes.